Refine Search

Search Results -

Terms	Documents
L5 near9 dynamic$6 near3 (configur$5 or program$5 or reconfigur$4 or reprogram$5) near4 controller	10

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L17

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Wednesday, July 07, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ			
L17	L5 near9 dynamic$6 near3 (configur$5 or program$5 or reconfigur$4 or reprogram$5) near4 controller	10	L17
L16	L5 near9 dynamic$6 near3 (configur$5 or program$5 or rconfigur$4 or reprogram$5) near4 controller	9	L16
L15	L6 same dynamic$5	23	L15
L14	L12 and monestime	1	L14
L13	L12 same exclus$5	1	L13
L12	fpga adj3 controller	322	L12
L11	fpga adj5 controller	470	L11
L10	L9 same l6	35	L10
L9	(plurality or multiple or more than one) near3 (task or operation)	97116	L9
L8	L6 same task$3 near3 (distribut$3 or schedul$3)	3	L8

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L7	L6 same media proces$4	1	L7
L6	L5 near9 (configur$5 or program$5 or rconfigur$4 or reprogram$5) near4 controller	809	L6
L5	(L4 or l3 or l2)	236596	L5
L4	(plurality or multiple or more than one) near3 ($5proces$sor or proces$4)	179955	L4
L3	(parallel or pipelin$3) near3 proces$4	79550	L3
L2	(parallel or pipelin$3) near3 $5processor	20731	L2
L1	(parallel or pipelin$3) near3 $5procesor	7	L1

END OF SEARCH HISTORY

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Hit List

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Search Results - Record(s) 1 through 10 of 10 returned.

☐ 1. Document ID: US 20040088459 A1

Using default format because multiple data bases are involved.

L17: Entry 1 of 10 File: PGPB May 6, 2004

PGPUB-DOCUMENT-NUMBER: 20040088459
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040088459 A1

TITLE: Shared peripheral architecture

PUBLICATION-DATE: May 6, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Gary, Sonya	Longmont	CO	US	
Tyger, Karen	Longmont	CO	US	

US-CL-CURRENT: 710/244

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D

☐ 2. Document ID: US 20030135547 A1

L17: Entry 2 of 10 File: PGPB Jul 17, 2003

DOCUMENT-IDENTIFIER: US 20030135547 A1
TITLE: Extensible modular communication executive with active message queue and intelligent message pre-validation

CLAIMS:

40. A data processing system configured to process spectral data generated by a plurality of remote sensing stations during sampling of unknown materials, the data processing system comprising: (a) an analysis engine configured to process spectral data to generate quantitative results therefrom using multivariate analysis; and (b) a communication executive interposed between the plurality of remote sensing stations and the analysis engine, the communication executive configured to communicate first spectral data generated by a first remote sensing station to the analysis engine, and to communicate first quantitative results from the analysis engine to the first remote sensing station subsequent to processing of the first spectral data by the analysis engine, the communication executive comprising: (i) a message buffer configured to receive messages including spectral data generated by

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the plurality of remote sensing stations; (ii) a plurality of processor components, each configured to perform a task associated with a message received by the message buffer, at least one processor component configured to access the analysis engine to initiate processing of spectral data by the analysis engine; (iii) a plurality of controller components, each configured to dynamically instantiate at least a subset of the plurality of processor components; and (iv) at least one delegator component configured to monitor the message buffer for messages, and in response to a first message associated with the first spectral data, to dynamically execute a controller component so as to initiate analysis of the first spectral data by the analysis engine and return the first quantitative results to the first remote sensing station.

☐ 3. Document ID: US 20020138225 A1

L17: Entry 3 of 10 File: PGPB Sep 26, 2002

DOCUMENT-IDENTIFIER: US 20020138225 A1
TITLE: Automatic configuration of delay parameters for memory controllers of slave processors

Cross Reference to Related Applications Paragraph:
[0001] This application is related to "Automatic Configuration of Delay Parameters in a Dynamic Memory Controller," concurrently filed herewith, and "A System of Connecting Multiple Processors in Cascade," concurrently filed herewith, the contents of both of which are incorporated by reference herein in their entirety.

☐ 4. Document ID: US 6760868 B2

L17: Entry 4 of 10 File: USPT Jul 6, 2004

DOCUMENT-IDENTIFIER: US 6760868 B2
TITLE: Diagnostic cage for testing redundant system controllers

CLAIMS:

1. A method of testing a computer system comprising: interconnecting a plurality of processing nodes; providing a primary system controller and a secondary system controller each for independently configuring said plurality of processing nodes into one or more dynamic system domains; logically isolating a given system domain formed by selected ones of said processing nodes from another system domain formed by other processing nodes; each of said processing nodes communicating with said primary and said secondary system controller via a node interface unit including a plurality of bus interfaces; operating said node interface unit in a caged mode by

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selectively isolating a given system controller and selected ones of said plurality of bus interfaces; wherein during operation in said caged mode said isolated given system controller performing a self-test and testing of a communication path between said isolated given system controller and said selected ones of said plurality of bus interfaces during operation of said one or more dynamic system domains.

2. The method as recited in claim 1 further comprising operating said secondary system controller in a stand-by mode while said primary system controller is configuring said plurality of processing nodes into one or more dynamic system domains.

5. Document ID: US 6662253 B1

L17: Entry 5 of 10 File: USPT Dec 9, 2003

DOCUMENT-IDENTIFIER: US 6662253 B1
TITLE: Shared peripheral architecture

CLAIMS:

8. The controller of claim 1 wherein the state value is dynamically configurable during operation by at least one of the plurality of processors.

6. Document ID: US 6604147 B1

L17: Entry 6 of 10 File: USPT Aug 5, 2003

DOCUMENT-IDENTIFIER: US 6604147 B1
TITLE: Scalable IP edge router

Abstract Text (1):
In a data communications network, an edge router comprises a buffer for storing data packets, one or more line interface cards for routing data packets to and from the data communications network, and a processing engine for processing a limited portion of each packet that has been captured by an associated line interface card in a packet tag. The processing engine includes one or more pipeline processing modules (PPMs) which may be dynamically configured by a system controller to perform specific processing functions in a pipelined arrangement. In order to increase edge router throughput, each packet tag is processed by the processing engine essentially in parallel with storage of the associated data packet in the

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buffer by the associated line interface card.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 7. Document ID: US 6425094 B1

L17: Entry 7 of 10 File: USPT Jul 23, 2002

DOCUMENT-IDENTIFIER: US 6425094 B1
TITLE: Diagnostic cage for testing redundant system controllers

CLAIMS:

1. A computer system comprising: a plurality of processing nodes including one or more processors interconnected by a network bus and configured to execute programmed instructions; and a primary system controller and a secondary system controller each coupled to independently configure said plurality of processing nodes into one or more dynamic system domains, wherein a given system domain formed by selected ones of said processing nodes is logically isolated from another system domain formed by other processing nodes; wherein each of said processing nodes further includes a node interface unit including a plurality of bus interfaces for communicating with said primary and said secondary system controller, wherein said node interface unit is configured to operate in a caged mode by selectively isolating a given system controller and selected ones of said plurality of bus interfaces; wherein said given system controller that is isolated during operation in said caged mode is configured to perform a self-test and testing of a communication path between said given system controller and said selected ones of said plurality of bus interfaces during operation of said one or more dynamic system domains.

2. The computer system as recited in claim 1, wherein said secondary system controller is further configured to operate in a stand-by mode while said primary system controller is configuring said plurality of processing nodes into one or more dynamic system domains.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 8. Document ID: US 6154186 A

L17: Entry 8 of 10 File: USPT Nov 28, 2000

DOCUMENT-IDENTIFIER: US 6154186 A
TITLE: Electronic entertainment and communication system

CLAIMS:

38. A passenger-based communications system for generating video displays on one of

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a plurality of passenger display units, comprising:

a controller;

a plurality of computer programs identifiable by program identifiers; and

a plurality of first data processors, each of the plurality of first data processors configured to execute at least one of the plurality of programs stored in its associated program receiving system to generate a video display on one of the passenger display units, the controller configured to dynamically assign each of the plurality of first data processors to one of the plurality of passenger display units,

wherein the controller is configured to indicate that one of the computer programs is to be executed by an assigned one of the first data processors.

☐ 9. Document ID: US 6145072 A

L17: Entry 9 of 10 File: USPT Nov 7, 2000

DOCUMENT-IDENTIFIER: US 6145072 A
TITLE: Independently non-homogeneously dynamically reconfigurable two dimensional interprocessor communication topology for SIMD multi-processors and apparatus for implementing same

Brief Summary Text (14):
The present invention is also embodied in a SIMD architecture having a two dimensional array of processing elements, with multiple chips containing the processing elements of the array, where a controller broadcasts instructions to all processing elements in the array, a dynamically reconfigurable switching means useful to connect four of the processing elements in the array into a group which may cross chip boundaries to form partitions with each partition associated with one chip, to direct data movement dynamically between selected processing elements of the group in accordance with either the broadcast instruction of the controller or a special communication instruction held in one processing element of the group. In this partitioned situation, the switch would include, in each partition, at least one dataline connected to each processing element in the group in the partition. A multiplexer unit is connected to each data line, the controller and to a configuration register. It is adapted to load the special communication instruction from the one processing element in the group into a configuration register and to operate in accord with either the broadcast instruction from the controller or the contents of the configuration register to select one of the four data lines as a source of data and applying the data therefrom to a source output port. A demultiplexer unit is connected to each data line, the controller, the configuration register, and to the source output port of the multiplexer unit. The demultiplexer is adapted to operate in accord with either the broadcast instruction from the controller or the contents of the configuration register to select one of the four data lines and applying the data from the source output port of the multiplexer thereto. A dataline connects each multiplexer in one partition to the demultiplexer in the same partition, and a crossing dataline connects each multiplexer in one partition to the demultiplexer in each other partition.

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CLAIMS:

6. In a SIMD architecture having a two dimensional array of processing elements, with multiple chips containing the processing elements of the array, where a controller broadcasts instructions to all processing elements in the array, a dynamically reconfigurable switching means useful to connect four of the processing elements in the array into a group which may cross chip boundaries to form partitions with each partition associated with one chip, to direct data movement dynamically between selected processing elements of the group in accordance with either the broadcast instruction of the controller or a special communication instruction held in one processing element of the group, the switch comprising in each partition:

at least one dataline connected to each processing element in the group in the partition;

a multiplexer means connected to each data line and to the controller and to a configuration register external to any processing element of the group, said configuration register controllable by any of the processing elements in the group, for loading the special communication instruction from one processing element in the group into the configuration register and to operate in accord with either the broadcast instruction from the controller or the contents of the configuration register to select one or none of the data lines in the partition as a source of data and applying the data therefrom to a source output port;

a demultiplexer means connected to each data line and to the controller and to said configuration register, and directly connected to the source output port of the multiplexer means, and for operating in response to the broadcast instruction from the controller or the contents of the configuration register to apply directly the data from the source output port of the multiplexer means to a selected one or none of the data lines in the partition; and

a dataline connecting each multiplexer in one partition to the demultiplexer in the same partition, and a crossing dataline connecting each multiplexer in one partition to the demultiplexer in each other partition.

☐ 10. Document ID: US 6112288 A

L17: Entry 10 of 10 File: USPT Aug 29, 2000

DOCUMENT-IDENTIFIER: US 6112288 A
TITLE: Dynamic configurable system of parallel modules comprising chain of chips comprising parallel pipeline chain of processors with master controller feeding command and data

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

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Terms	Documents
L5 near9 dynamic$6 near3 (configur$5 or program$5 or reconfigur$4 or reprogram$5) near4 controller	10

Display Format: - Change Format

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Search Results - Record(s) 1 through 23 of 23 returned.

☐ 1. Document ID: US 20030135547 A1

Using default format because multiple data bases are involved.

L15: Entry 1 of 23 File: PGPB Jul 17, 2003

PGPUB-DOCUMENT-NUMBER: 20030135547
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030135547 A1

TITLE: Extensible modular communication executive with active message queue and intelligent message pre-validation

PUBLICATION-DATE: July 17, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Kent, J. Thomas	Cincinnati	OH	US	
Toot, David A.	Mason	OH	US	

US-CL-CURRENT: 709/203

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D

☐ 2. Document ID: US 6760868 B2

L15: Entry 2 of 23 File: USPT Jul 6, 2004

DOCUMENT-IDENTIFIER: US 6760868 B2
TITLE: Diagnostic cage for testing redundant system controllers

CLAIMS:

1. A method of testing a computer system comprising: interconnecting a plurality of processing nodes; providing a primary system controller and a secondary system controller each for independently configuring said plurality of processing nodes into one or more dynamic system domains; logically isolating a given system domain formed by selected ones of said processing nodes from another system domain formed by other processing nodes; each of said processing nodes communicating with said primary and said secondary system controller via a node interface unit including a plurality of bus interfaces; operating said node interface unit in a caged mode by selectively isolating a given system controller and selected ones of said plurality of bus interfaces; wherein during operation in said caged mode said isolated given system controller performing a self-test and testing of a communication path

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between said isolated given system controller and said selected ones of said plurality of bus interfaces during operation of said one or more dynamic system domains.

2. The method as recited in claim 1 further comprising operating said secondary system controller in a stand-by mode while said primary system controller is configuring said plurality of processing nodes into one or more dynamic system domains.

☐ 3. Document ID: US 6604147 B1

L15: Entry 3 of 23 File: USPT Aug 5, 2003

DOCUMENT-IDENTIFIER: US 6604147 B1
TITLE: Scalable IP edge router

Abstract Text (1):
In a data communications network, an edge router comprises a buffer for storing data packets, one or more line interface cards for routing data packets to and from the data communications network, and a processing engine for processing a limited portion of each packet that has been captured by an associated line interface card in a packet tag. The processing engine includes one or more pipeline processing modules (PPMs) which may be dynamically configured by a system controller to perform specific processing functions in a pipelined arrangement. In order to increase edge router throughput, each packet tag is processed by the processing engine essentially in parallel with storage of the associated data packet in the buffer by the associated line interface card.

☐ 4. Document ID: US 6425094 B1

L15: Entry 4 of 23 File: USPT Jul 23, 2002

DOCUMENT-IDENTIFIER: US 6425094 B1
TITLE: Diagnostic cage for testing redundant system controllers

CLAIMS:

1. A computer system comprising: a plurality of processing nodes including one or more processors interconnected by a network bus and configured to execute programmed instructions; and a primary system controller and a secondary system controller each coupled to independently configure said plurality of processing nodes into one or more dynamic system domains, wherein a given system domain formed by selected ones of said processing nodes is logically isolated from another system

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domain formed by other processing nodes; wherein each of said processing nodes further includes a node interface unit including a plurality of bus interfaces for communicating with said primary and said secondary system controller, wherein said node interface unit is configured to operate in a caged mode by selectively isolating a given system controller and selected ones of said plurality of bus interfaces; wherein said given system controller that is isolated during operation in said caged mode is configured to perform a self-test and testing of a communication path between said given system controller and said selected ones of said plurality of bus interfaces during operation of said one or more dynamic system domains.

2. The computer system as recited in claim 1, wherein said secondary system controller is further configured to operate in a stand-by mode while said primary system controller is configuring said plurality of processing nodes into one or more dynamic system domains.

☐ 5. Document ID: US 6263396 B1

L15: Entry 5 of 23 File: USPT Jul 17, 2001

DOCUMENT-IDENTIFIER: US 6263396 B1
TITLE: Programmable interrupt controller with interrupt set/reset register and dynamically alterable interrupt mask for a single interrupt processor

Abstract Text (1):
A programmable interrupt controller (510) for a single interrupt architecture processor (518) includes a plurality of interrupt sources (502) each operable to generate an interrupt. A dynamically alterable interrupt mask (508) selectively blocks interrupt signals for the interrupt sources (502). Interrupts permitted by the dynamically alterable interrupt mask (508) are processed by an interrupt handler (500) for the single interrupt architecture processor (518) in order of priority. In addition, processing for a lower priority interrupt is interrupted in order to process a later received higher priority interrupt permitted by the dynamically alterable interrupt mask (508).

Brief Summary Text (30):
In accordance with one embodiment of the present invention, a programmable interrupt controller for a single interrupt architecture processor includes a plurality of interrupt sources each operable to generate an interrupt. A dynamically alterable interrupt mask selectively blocks interrupt signals for the interrupt sources. Interrupts permitted by the dynamically alterable interrupt mask are processed by an interrupt handler for the single interrupt architecture processor in order of priority. In addition, processing for a lower priority interrupt is interrupted in order to process a later received higher priority interrupt permitted by the dynamically alterable interrupt mask.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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☐ 6. Document ID: US 6241404 B1

L15: Entry 6 of 23 File: USPT Jun 5, 2001

DOCUMENT-IDENTIFIER: US 6241404 B1
TITLE: Method for controlling the flow of paper objects in a paper processing system

Brief Summary Text (8):
Published European patent application EP-A2-0 778 523 discloses a method of operation of an image processing apparatus having a controller and a plurality of resources arranged in an arbitrary configuration. Each of the resources provides an associated processor storing data related to operational capabilities of the associated resource. The controller is adapted to dynamically configure the image processing apparatus to operate in accordance with the operational capabilities of each of the processors by defining job requirements as a combination of images defining a set of sheets and specifying compilations of sheets.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 7. Document ID: US 6175358 B1

L15: Entry 7 of 23 File: USPT Jan 16, 2001

DOCUMENT-IDENTIFIER: US 6175358 B1
TITLE: Gameport communication apparatus and method

Detailed Description Text (3):
FIG. 1 depicts components of a computer system generally of the type known as a 486 computer. As shown in FIG. 1, the computer system includes a microprocessor 102 coupled to a plurality of controllers and peripherals, which are optional, depending on the system configuration. The microprocessor includes a bus interface 104 for interfacing with, e.g., mass storage units and peripherals. An address drivers 104a provides proper addresses on the address bus of the proper level for storing and transmitting information including program information and data to and from a conventional memory, such as dynamic random access memory (DRAM) 108, e.g., via a DRAM controller 108b or a direct memory access (DMA) controller 108b, or to and from a hard drive 110, via a hard drive controller 110a or a floppy drive 112 via a floppy drive controller 112a, or to or from network storage over a local area network (LAN) 114 via a network controller 114a or to or from other data sources and sinks such as remote devices, e.g., via a modem (optional), e.g., for Internet access or communications with other network systems, a mouse or keyboard 122, via keyboard interface 120, or a joystick 123a via a joystick or game card or controller 123b.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw D

☐ 8. Document ID: US 6154186 A

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L15: Entry 8 of 23 File: USPT Nov 28, 2000

DOCUMENT-IDENTIFIER: US 6154186 A
TITLE: Electronic entertainment and communication system

CLAIMS:

38. A passenger-based communications system for generating video displays on one of a plurality of passenger display units, comprising:

a controller;

a plurality of computer programs identifiable by program identifiers; and

a plurality of first data processors, each of the plurality of first data processors configured to execute at least one of the plurality of programs stored in its associated program receiving system to generate a video display on one of the passenger display units, the controller configured to dynamically assign each of the plurality of first data processors to one of the plurality of passenger display units,

wherein the controller is configured to indicate that one of the computer programs is to be executed by an assigned one of the first data processors.

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 9. Document ID: US 6112288 A

L15: Entry 9 of 23 File: USPT Aug 29, 2000

DOCUMENT-IDENTIFIER: US 6112288 A
TITLE: Dynamic configurable system of parallel modules comprising chain of chips comprising parallel pipeline chain of processors with master controller feeding command and data

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw D

☐ 10. Document ID: US 5999990 A

L15: Entry 10 of 23 File: USPT Dec 7, 1999

DOCUMENT-IDENTIFIER: US 5999990 A
TITLE: Communicator having reconfigurable resources

Abstract Text (1):

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A communicator (10) includes a plurality of reconfigurable resource units (13) that can each be dynamically altered to perform any of a multitude of processing tasks. A controller (16) determines a plurality of processing tasks to be supported by the communicator (10) and configures the plurality of reconfigurable resource units (13) accordingly. A memory (18) stores a library of configuration files for use by the controller (16) in configuring the plurality of reconfigurable resource units (13). In one embodiment, the controller (16) continuously adapts the plurality of reconfigurable resource units (13) according to present system requirements.

☐ 11. Document ID: US 5985357 A

L15: Entry 11 of 23 File: USPT Nov 16, 1999

DOCUMENT-IDENTIFIER: US 5985357 A
TITLE: Treating solution supplying method and apparatus

Detailed Description Text (33):
In successively executing the plurality of instructions included in the processing program, the controller 20 selects a course of action by determining whether the instruction is a supply start instruction to deliver the photoresist solution from the treating solution supply nozzle 5. In the "static method", the instruction executed first is the supply start instruction, and the operation proceeds to step S3. In the "dynamic method" described hereinafter, the first instruction is the spin start instruction, and therefore the operation proceeds to step S2 to execute the spin start instruction.

☐ 12. Document ID: US 5811940 A

L15: Entry 12 of 23 File: USPT Sep 22, 1998

DOCUMENT-IDENTIFIER: US 5811940 A
TITLE: Phase-shift lamp control

Detailed Description Text (21):
If control elements with a control program produced individually for each tube are now allocated to each tube of a lighting system and if the control programs take place synchronously with one another in the individual control elements, a multiprocessor controller with parallel processing is created with which even very complex and highly dynamic light and colour structures can be controlled for the entire system. For synchronisation, the a.c. operating voltage serves as a clock signal to which all lamps are connected in parallel. The program start is synchronized via the power on reset logic provided in every signal processor.

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☐ 13. Document ID: US 5778413 A

L15: Entry 13 of 23 File: USPT Jul 7, 1998

DOCUMENT-IDENTIFIER: US 5778413 A
TITLE: Programmable memory controller having two level look-up for memory timing parameter

Abstract Text (1):
A memory controller which provides a series of queues between the processor and the PCI bus and the memory system. Memory coherency is maintained in two different ways. Before any read operations are accepted from the PCI bus, both of the posting queues must be empty. A content addressable memory (CAM) is utilized as the Peripheral Component Interconnect (PCI) to memory queue. When the processor performs a read request, the CAM is checked to determine if one of the pending write operations in the PCI to memory queue is to the same address as the read operation of the processor. If so, the read operation is not executed until the PCI memory queue is cleared of the write. To resolve the problem of aborting a Memory Read Multiple operation, an abort signal from the PCI bus interface is received and as soon thereafter as can be done the read ahead cycle is terminated, even though the read ahead cycle has not fully completed. The memory controller has improved prediction rules based on whether the cycle is coming from the processor or is coming from the PCI bus to allow more efficient precharging when PCI bus cycles are used. The memory controller is highly programmable for multiple speeds and types of processors and several speeds of memory devices. The memory controller includes a plurality of registers that specify number of clock periods for the particular portions of a conventional dynamic random access memory cycle which are used to control state machine operations.

☐ 14. Document ID: US 5714981 A

L15: Entry 14 of 23 File: USPT Feb 3, 1998

DOCUMENT-IDENTIFIER: US 5714981 A
TITLE: Gameport communication apparatus and method

Detailed Description Text (3):
FIG. 1 depicts components of a computer system generally of the type known as a 486 computer. As shown in FIG. 1, the computer system includes a microprocessor 102 coupled to a plurality of controllers and peripherals, which are optional, depending on the system configuration. The microprocessor includes a bus interface 104 for interfacing with, e.g., mass storage units and peripherals. An address driver 104a provides proper addresses on the address bus of the proper level for storing and transmitting information including program information and data to and from a conventional memory, such as dynamic random access memory (DRAM) 108, e.g., via a DRAM controller 108b or a direct memory access (DMA) controller 108b, or to and from a hard drive 110, via a hard drive controller 110a or a floppy drive 112 via a floppy drive controller 112a, or to or from network storage over a local area

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network (LAN) 114 via a network controller 114a or to or from other data sources and sinks such as remote devices, e.g., via a modem (optional), e.g., for Internet access or communications with other network systems. a mouse or keyboard 122, via keyboard interface 120, or a joystick 123a via a joystick or game card or controller 123b.

☐ 15. Document ID: US 5701557 A

L15: Entry 15 of 23 File: USPT Dec 23, 1997

DOCUMENT-IDENTIFIER: US 5701557 A
TITLE: Machine graphs and capabilities to represent document output terminals composed of arbitrary configurations

Abstract Text (1):
An electronic image processing apparatus has a controller and a plurality of resources in an arbitrary configuration. Each of the resources includes an associated processor storing data related to operational constraints of the associated resource and a bus interconnects the processors to the controller for directing the operation of the resources. The controller is adapted to operate independent of a particular configuration of the plurality of resources by receiving from each of the processors the data related to the operational constraints of each associated resource and interrogating each of the processors to determine the geometrical relationship of the interconnection of the resources. The controller then responds to the data related to the operational constraints of each of the processors and to the geometrical relationship of the interconnection of the resources to dynamically configure the image processing apparatus to operate in accordance with the the operational constraints of each of the processors and to the geometrical relationship of the interconnection of the resources.

Brief Summary Text (15):
According to the present invention, an electronic image processing apparatus is provided with a controller and a plurality of resources in an arbitrary configuration. Each of the resources includes an associated processor storing data related to operational constraints of the associated resource and a bus interconnects the processors to the controller for directing the operation of the resources. The controller is adapted to operate independent of a particular configuration of the plurality of resources by receiving from each of the processors the data related to the operational constraints of each associated resource and interrogating each of the processors to determine the geometrical relationship of the interconnection of the resources. The controller then responds to the data related to the operational constraints of each of the processors and to the geometrical relationship of the interconnection of the resources to dynamically configure the image processing apparatus to operate in accordance with the operational constraints of each of the processors and to the geometrical relationship of the interconnection of the resources.

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☐ 16. Document ID: US 5646740 A

L15: Entry 16 of 23 File: USPT Jul 8, 1997

DOCUMENT-IDENTIFIER: US 5646740 A
TITLE: Partial or untimed production trees to specify diagnostics operations requiring multiple module cooperation

Brief Summary Text (16):
According to the present invention, an electronic image processing apparatus is provided with a controller and a plurality of resources in an arbitrary configuration. Each of the resources includes an associated processor storing data related to operational capabilities of the associated resource. The controller is adapted to dynamically configure the image processing apparatus to operate in accordance with the operational capabilities of each of the processors and to define processing requirements as a combination of images defining a set of sheets and specifying compilations of sheets. The processing requirement is converted into an assembly tree relationship for merging into additional assembly trees for formulating the job requirement. The controller responds to the data related to the operational capabilities of each of the modules and to the the assembly tree relationship of images, copy sheets, and compilations of copy sheets for providing a production tree relationship of the operational capabilities of the modules including timing relationships for operating the image processing apparatus. The production tree relationship further permits arbitrary definition of a job requirement into a first segment independent of the capabilities of the modules and a second segment dependent upon selected capabilities of selected modules to allow the image processing apparatus to be partially configured based upon operator entered constraints. This technique further allows adaptive control of selective diagnostics.

☐ 17. Document ID: US 5631740 A

L15: Entry 17 of 23 File: USPT May 20, 1997

DOCUMENT-IDENTIFIER: US 5631740 A
TITLE: Transducers with constraints model for print scheduling

Abstract Text (1):
An electronic image processing apparatus has a controller and a plurality of resources in an arbitrary configuration. Each of the resources includes an associated processor storing data related to operational constraints of the associated resource and a bus interconnects the processors to the controller for directing the operation of the resources. The controller is adapted to operate independent of a particular configuration of the plurality of resources by receiving from each of the processors the data related to the operational constraints of each associated resource and interrogating each of the processors to determine the geometrical relationship of the interconnection of the resources. The controller then responds to the data related to the operational constraints of each of the processors and to the geometrical relationship of the interconnection of the resources to dynamically configure the image processing apparatus to operate in

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accordance with the the operational constraints of each of the processors and to the geometrical relationship of the interconnection of the resources.

Brief Summary Text (15):
According to the present invention, an electronic image processing apparatus is provided with a controller and a plurality of resources in an arbitrary configuration. Each of the resources includes an associated processor storing data related to operational constraints of the associated resource and a bus interconnects the processors to the controller for directing the operation of the resources. The controller is adapted to operate independent of a particular configuration of the plurality of resources by receiving from each of the processors the data related to the operational constraints of each associated resource and interrogating each of the processors to determine the geometrical relationship of the interconnection of the resources. The controller then responds to the data related to the operational constraints of each of the processors and to the geometrical relationship of the interconnection of the resources to dynamically configure the image processing apparatus to operate in accordance with the the operational constraints of each of the processors and to the geometrical relationship of the interconnection of the resources.

☐ 18. Document ID: US 5617215 A

L15: Entry 18 of 23 File: USPT Apr 1, 1997

DOCUMENT-IDENTIFIER: US 5617215 A
TITLE: Assembly trees for canonical representation of documents and blending multiple functions

Brief Summary Text (16):
According to the present invention, an electronic image processing apparatus is provided with a controller and a plurality of resources in an arbitrary configuration. Each of the resources includes an associated processor storing data related to operational capabilities of the associated resource. The controller is adapted to dynamically configure the image processing apparatus to operate in accordance with the operational capabilities of each of the processors and to define processing requirements as a combination of images defining a set of sheets and specifying compilations of sheets. The processing requirement is converted into an assembly tree relationship for merging into additional assembly trees for formulating the job requirement. The controller responds to the data related to the operational capabilities of each of the modules and to the the assembly tree relationship of images, copy sheets, and compilations of copy sheets for providing a production tree relationship of the operational capabilities of the modules including timing relationships for operating the image processing apparatus. The production tree relationship further permits arbitrary definition of a job requirement into a first segment independent of the capabilities of the modules and a second segment dependent upon selected capabilities of selected modules to allow the image processing apparatus to be partially configured based upon operator entered constraints. This technique further allows adaptive control of selective diagnostics.

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw De

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☐ 19. Document ID: US 5617214 A

L15: Entry 19 of 23 File: USPT Apr 1, 1997

DOCUMENT-IDENTIFIER: US 5617214 A
TITLE: Commitment groups to generalize the scheduling of interdependent document output terminal capabilities

Abstract Text (1):
An electronic image processing apparatus has a controller and a plurality of resources in an arbitrary configuration. Each of the resources includes an associated processor storing data related to operational constraints of the associated resource and a bus interconnects the processors to the controller for directing the operation of the resources. The controller is adapted to operate independent of a particular configuration of the plurality of resources by receiving from each of the processors the data related to the operational constraints of each associated resource and interrogating each of the processors to determine the geometrical relationship of the interconnection of the resources. The controller then responds to the data related to the operational constraints of each of the processors and to the geometrical relationship of the interconnection of the resources to dynamically configure the image processing apparatus to operate in accordance with the the operational constraints of each of the processors and to the geometrical relationship of the interconnection of the resources.

Brief Summary Text (15):
According to the present invention, an electronic image processing apparatus is provided with a controller and a plurality of resources in an arbitrary configuration. Each of the resources includes an associated processor storing data related to operational constraints of the associated resource and a bus interconnects the processors to the controller for directing the operation of the resources. The controller is adapted to operate independent of a particular configuration of the plurality of resources by receiving from each of the processors the data related to the operational constraints of each associated resource and interrogating each of the processors to determine the geometrical relationship of the interconnection of the resources. The controller then responds to the data related to the operational constraints of each of the processors and to the geometrical relationship of the interconnection of the resources to dynamically configure the image processing apparatus to operate in accordance with the the operational constraints of each of the processors and to the geometrical relationship of the interconnection of the resources.

☐ 20. Document ID: US 5604600 A

L15: Entry 20 of 23 File: USPT Feb 18, 1997

DOCUMENT-IDENTIFIER: US 5604600 A
TITLE: Production trees for generic representation of document requirements for particular output terminals

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Brief Summary Text (16):
According to the present invention, an electronic image processing apparatus is provided with a controller and a plurality of resources in an arbitrary configuration. Each of the resources includes an associated processor storing data related to operational capabilities of the associated resource. The controller is adapted to dynamically configure the image processing apparatus to operate in accordance with the operational capabilities of each of the processors and to define processing requirements as a combination of images defining a set of sheets and specifying compilations of sheets. The processing requirement is converted into an assembly tree relationship for merging into additional assembly trees for formulating the job requirement. The controller responds to the data related to the operational capabilities of each of the modules and to the the assembly tree relationship of images, copy sheets, and compilations of copy sheets for providing a production tree relationship of the operational capabilities of the modules including timing relationships for operating the image processing apparatus. The production tree relationship further permits arbitrary definition of a job requirement into a first segment independent of the capabilities of the modules and a second segment dependent upon selected capabilities of selected modules to allow the image processing apparatus to be partially configured based upon operator entered constraints. This technique further allows adaptive control of selective diagnostics.

☐ 21. Document ID: US 5559606 A

L15: Entry 21 of 23 File: USPT Sep 24, 1996

DOCUMENT-IDENTIFIER: US 5559606 A
TITLE: Flexible configuration of document output terminals from autonomous machine modules

Abstract Text (1):
An electronic image processing apparatus has a controller and a plurality of resources in an arbitrary configuration. Each of the resources includes an associated processor storing data related to operational constraints of the associated resource and a bus interconnects the processors to the controller for directing the operation of the resources. The controller is adapted to operate independent of a particular configuration of the plurality of resources by receiving from each of the processors the data related to the operational constraints of each associated resource and interrogating each of the processors to determine the geometrical relationship of the interconnection of the resources. The controller then responds to the data related to the operational constraints of each of the processors and to the geometrical relationship of the interconnection of the resources to dynamically configure the image processing apparatus to operate in accordance with the the operational constraints of each of the processors and to the geometrical relationship of the interconnection of the resources.

Brief Summary Text (15):
According to the present invention, an electronic image processing apparatus is provided with a controller and a plurality of resources in an arbitrary configuration. Each of the resources includes an associated processor storing data related to operational constraints of the associated resource and a bus interconnects the processors to the controller for directing the operation of the

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resources. The controller is adapted to operate independent of a particular configuration of the plurality of resources by receiving from each of the processors the data related to the operational constraints of each associated resource and interrogating each of the processors to determine the geometrical relationship of the interconnection of the resources. The controller then responds to the data related to the operational constraints of each of the processors and to the geometrical relationship of the interconnection of the resources to dynamically configure the image processing apparatus to operate in accordance with the the operational constraints of each of the processors and to the geometrical relationship of the interconnection of the resources.

☐ 22. Document ID: US 4351023 A

L15: Entry 22 of 23 File: USPT Sep 21, 1982

DOCUMENT-IDENTIFIER: US 4351023 A
TITLE: Process control system with improved system security features

Brief Summary Text (6):
Keiles discloses a process control system that includes a plurality of primary process controllers, with each having stored in its random access memory (RAM) configuration information that is compatible with the type of control function being performed by the particular controller. There is also disclosed a single backup controller arranged to be substituted for a failed primary. However, since Keiles' backup is not being used for monitoring and controlling the process, its RAM is devoid of any configuration information, and accordingly upon failure of a primary, the RAM of the primary controller is transferred to the RAM of the backup to allow it to assume the identity of the failed controller. Although not entirely clear from the disclosure, it does not appear that Keiles is concerned with automatically preserving dynamic (i.e., current process input/output values, results of time dependent calculations, etc.) state information in addition to the static (i.e., configuration) information. Furthermore, there is a high likelihood that the data base will be corrupted if controller failure occurs while updating this information.

☐ 23. Document ID: EP 707268 A2

L15: Entry 23 of 23 File: EPAB Apr 17, 1996

PUB-NO: EP000707268A2
DOCUMENT-IDENTIFIER: EP 707268 A2
TITLE: Easily programmable memory controller which can access different speed memory devices on different cycles

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